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W. H. Chen

Very Low Defects and High Performance Ge-On-Insulator p-MOSFETs with Al₂O₃ Gate Dielectrics

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Abstract

We demonstrate for the first time high quality and dislocation free Ge-on-insulator (GOI) p-MOSFETs with Al₂O₃ gate dielectrics [EOT=1.7nm]. Compared to control Al₂O₃/Si p-MOSFETs, the Al₂O₃/GOI devices show similar leakage current for the same EOT, 2X increase in drive current, and 2.5X increase in hole mobility. In addition, the Al₂O₃/GOI devices exhibit 1.3X enhanced hole mobility over the SiO₂/Si universal hole mobility at E_{eff} of 1MV/cm.

Introduction

Pure Ge channel MOSFETs have attracted much attention due to its enhanced electron and hole mobility over conventional Si-MOSFET [1]. These improvements are especially important for high-k gate dielectric MOSFETs where the mobility degradation is the main technology bottleneck. Both strained and relaxed Ge channel and Ge bulk p-MOSFETs have recently been reported [2]-[3]. In this paper, we demonstrate for the first time high quality and dislocation free Ge-on-insulator (GOI) p-MOSFETs with Al₂O₃ gate dielectrics [4]. This low defects are mandatory for real VLSI manufacture (<1 dislocation/cm²) to achieve a high yield. In addition to the orders of magnitude lower defect density than strained Si or relaxed SiGe on Si, the Al₂O₃/GOI devices show similar leakage current for the same EOT, 2X increase in drive current, and 2.5X increase in hole mobility compared to control Al₂O₃/Si p-MOSFETs. In addition, the Al₂O₃/GOI devices exhibit 1.3X enhancement of hole mobility over the SiO₂/Si universal mobility.

Experimental

After depositing 75 nm SiO₂ on Ge and Si wafers, the GOI was formed by bonding SiO₂/Ge and SiO₂/Si at 500°C for 10 hrs. To enhance the bonding at such low temperature, O₂ plasma was used to activate the SiO₂ surface before bonding [5] and a constant pressure was applied during bonding process. After etch back, a 400nm isolation SiO₂ was deposited on Ge. The p⁺ source and drain were formed by implanting B⁺, followed by 500°C furnace anneal. Al₂O₃ gate dielectric [4] was deposited on Ge, followed by Al gate electrode formation. For comparison, Al₂O₃/Si_{0.3}Ge_{0.7} and Al₂O₃/Si p-MOSFETs were also fabricated, where a solid-phase epitaxy was used to form the Si_{0.3}Ge_{0.7} on Si [3].

Results and Discussion

A. GOI characterization

Fig. 1 shows the X TEM of GOI wafer. The different contrast between top and bottom layers is due to the different electron scattering of Ge and Si atoms and small crystal orientation misalignment. No defect can be observed on top.

Ge. To our knowledge, this is the first demonstration of defect free GOI structure. The GOI structure was further characterized by Energy Dispersive Spectroscopy (EDS) shown in Fig. 2, and a Ge layer on SiO₂/Si was confirmed. An interfacial layer at the bonding interface and middle of SiO₂ is due to the O₂ plasma treatment [5]. Very smooth Ge/SiO₂ interface, comparable SOI, is achieved, and is essential for ultra-thin body GOI MOSFET.

B. Al₂O₃/GOI capacitor and reliability

Figs. 3 and 4 present the respective J-V and C-V characteristics of Al₂O₃ capacitors on GOI, Si_{0.3}Ge_{0.7}/Si, and Si substrates. Comparable leakage current is observed for these devices with similar EOT=1.7nm from C-V measurement. A Jg=1.5×10⁻³ A/cm² at 1V for Al₂O₃/GOI with EOT=1.7nm is 3 orders of magnitude lower than that in SiO₂/Si. Good reliability for Al₂O₃/GOI gate dielectric is evidenced from the high t_{BD} and MTF, as shown in Fig. 5, and is comparable to Al₂O₃/Si devices. An extrapolated max operating voltage of 2.5V is obtained for 10 years lifetime.

C. Al₂O₃/GOI p-MOSFET and mobility

Figs. 6 and 7 show the I_d-V_d of Al₂O₃/Si_{0.3}Ge_{0.7}/Si and Al₂O₃/GOI, respectively, and the control Al₂O₃/Si device is also shown in Fig. 6. Significant enhancement in I_d for both Al₂O₃/GOI and Al₂O₃/Si_{0.3}Ge_{0.7}/Si over Al₂O₃/Si devices is observed, with the Al₂O₃/GOI device showing the highest I_d. The relatively large I_{d,OFF} shown in Fig. 8 can be improved by thinning down the top Ge layer. The effective mobility is plotted in Fig. 9. As can be seen clearly, the hole mobility increases with increasing Ge content, where the mobility for Al₂O₃/Si_{0.3}Ge_{0.7}/Si and Al₂O₃/GOI are 1.7X and 2.5X, respectively, higher than Al₂O₃/Si control device at E_{eff} of 1.0MV/cm. The hole mobility is also 1.3X higher than the published universal mobility data from thermal SiO₂/Si at 1MV/cm E_{eff}.

Conclusions

We have demonstrated for the first time a defect free GOI structure and a high performance Ge p-MOSFET with Al₂O₃ gate dielectric (EOT=1.7nm). Results show that Al₂O₃/GOI p-MOSFET has low gate leakage current of 1.5×10⁻³ A/cm² at 1V and 2.5X enhancement in hole mobility over control Al₂O₃/Si devices. In addition, the Al₂O₃/GOI devices exhibit 1.3X enhancement of hole mobility over the SiO₂/Si universal mobility at E_{eff} of 1MV/cm.

References

- [1] C. O. Chui et al, *IEDM Tech. Dig.* (2002), p. 437.
- [2] J. Hoyt et al, *IEDM Tech. Dig.* (2002), p. 23.
- [3] Y. H. Wu and A. Chin, *IEEE EDL* 21, p. 350 (2000).
- [4] A. Chin et al, *Symp. On VLSI Tech.* (1999), p. 135.
- [5] Y. H. Wu et al, *J. Electrochemical Soc.* 147, p. 2254 (2000).

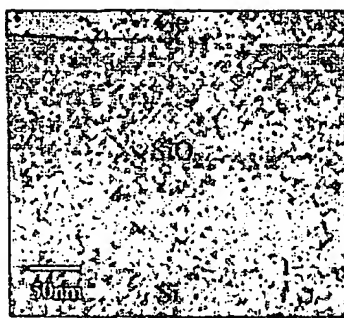


Fig. 1. Cross-sectional TEM of GOI. The different contrast between the top Ge and bottom Si substrate is due to the different atomic scattering of electron beams and small crystal orientation misalignment. No dislocations can be observed in GOI.

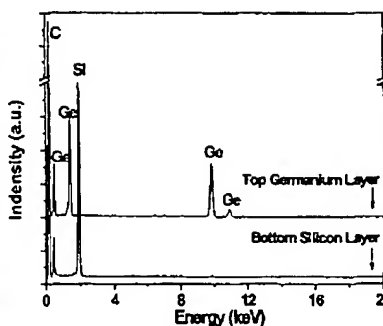


Fig. 2. The measured Energy Dispersive Spectroscopy from top and bottom layers, which confirms the GOI structure shown in Fig. 1. The Carbon signal is from the glue.

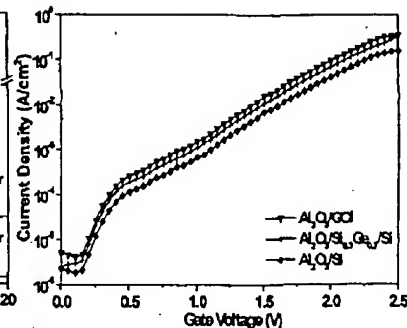


Fig. 3. The measured J-V characteristics of Al_2O_3 gate dielectric on GOI, $\text{Si}_0.3\text{Ge}_0.7/\text{Si}$ and Si. The comparable gate leakage current indicates that high quality Al_2O_3 gate dielectric can be formed on GOI.

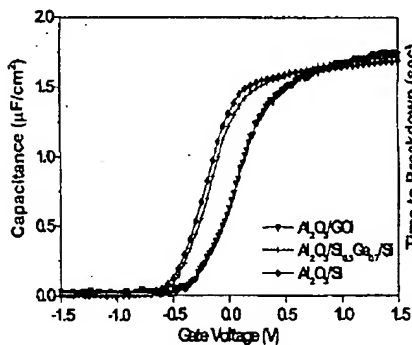


Fig. 4. The 1MHz C-V characteristics of Al_2O_3 gate dielectric on GOI, $\text{Si}_0.3\text{Ge}_0.7/\text{Si}$ and Si. A k value of 9 and EOT of 1.7nm are obtained.

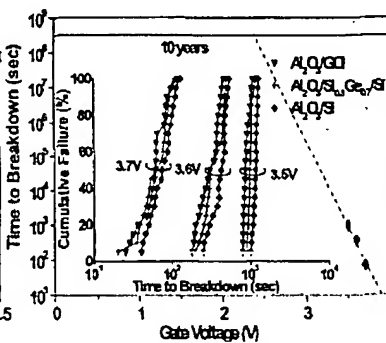


Fig. 5. The measured and extrapolated Mean-Time to Failure MTTF as a function of gate voltage from the inserted dielectric breakdown time t_{BD} distribution plot.

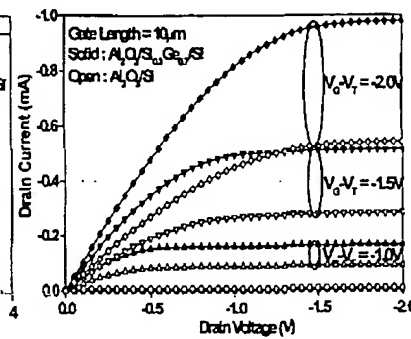


Fig. 6. The I_d - V_d characteristics of $\text{Al}_2\text{O}_3/\text{Si}_0.3\text{Ge}_0.7/\text{Si}$ and $\text{Al}_2\text{O}_3/\text{Si}$ p-MOSFETs. At the same V_g - V_t , the I_d from $\text{Al}_2\text{O}_3/\text{Si}_0.3\text{Ge}_0.7/\text{Si}$ device is 1.8X higher than $\text{Al}_2\text{O}_3/\text{Si}$ control p-MOSFETs.

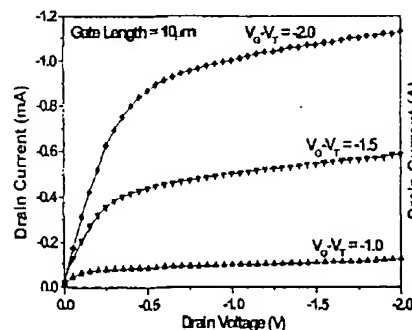


Fig. 7. The I_d - V_d characteristics of $\text{Al}_2\text{O}_3/\text{GOI}$ PMOSFETs. At the same V_g - V_t , the I_d from $\text{Al}_2\text{O}_3/\text{GOI}$ device is 2.0X higher than $\text{Al}_2\text{O}_3/\text{Si}$ control p-MOSFETs in Fig. 6.

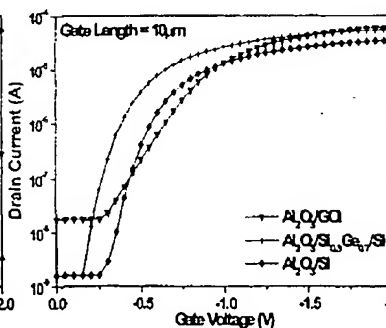


Fig. 8. The I_d - V_g characteristics of $\text{Al}_2\text{O}_3/\text{GOI}$, $\text{Al}_2\text{O}_3/\text{Si}_0.3\text{Ge}_0.7/\text{Si}$ and $\text{Al}_2\text{O}_3/\text{Si}$ p-MOSFETs. At the same 10μm gate length, the I_d from $\text{Al}_2\text{O}_3/\text{GOI}$ device is the highest than others that is due to the highest Ge%.

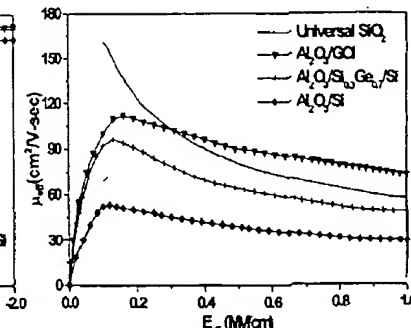


Fig. 9. The hole mobility of $\text{Al}_2\text{O}_3/\text{GOI}$, $\text{Al}_2\text{O}_3/\text{Si}_0.3\text{Ge}_0.7/\text{Si}$ and $\text{Al}_2\text{O}_3/\text{Si}$ p-MOSFETs. The hole mobility increases with increasing Ge content and is higher than the universal SiO_2/Si hole mobility at GOI device.